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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/797,804

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Steven E. Boor

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EXAMINER

OLANIRAN, FATIMAT O

ART UNIT

PAPER NUMBER

2614

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DELIVERY MODE

02/18/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/797,804

Applicant(s)

BOOR, STEVEN E.

Examiner

FATIMAT O. OLANIRAN

Art Unit

2614

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 November 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 and 13-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10, 13-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/24/2008 have been fully considered but they are not persuasive.

2. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant argues on pg 7 par 2, "...Contrary to claim 1, Levitt does not teach or suggest a transducer housing and a hybrid circuit in the transducer housing. For example, the FIG. 2 of Levitt illustrates the hearing aid that contains a microphone 57 and the circuit parts: automatic gain control (AGC) 58, a hearing aid amplifier 60, a hearing aid filter 63, a hearing aid programmable filter 64, and an EEPROM 84 (Col. 3, 11.39-41 and Col. 11, 11.41 and 42, and 11.48-52). None of these circuit parts are fitted in the housing of the microphone 57. In fact, Levitt does not disclose the microphone housing at all. Therefore, Levitt cannot be said to teach or suggest the subject matter of claim 1."

Examiner respectfully disagrees; the wearable hearing aid is the housing of the microphone. In addition applicant claim 1 is directed toward, "...A transducer assembly

comprising..." (preamble of claim 1) not a single transducer and not specifically a microphone.

Applicant argues, pg 7 par 3, "...Levitt has many additional deficiencies. For example, Levitt does not teach or suggest a hybrid circuit having a removable portion external to the transducer housing. The action has identified as a programming slot 124 (action, page 4, point 4, lines 10 and 11) as corresponding to the recited removable portion of claim 1. Levitt merely describes a host controller 20 that includes a programming slot 124 (Col. 8, 11.8 and 29). This programming slot 124 or the host controller 20 is not part of the hearing aid circuit at all. In fact, the host controller 20 is a bus interface that forms as part of a computer adapted to connect the computer to the hearing aid for reducing acoustic feedback (FIG. 1 and Col. 8, 11.25-29). There is no teaching by Levitt that the host controller circuit and the hearing aid circuit are on the same circuit board. Therefore, Levitt cannot be said to teach or suggest that a microphone hybrid circuit having a removable portion. It would be necessary for Levitt to describe one part of the circuit as being partially enclosed in the microphone housing and the remaining part of the circuit being the removal portion external to the microphone housing for it to teach or suggest these limitations of claim 1. For these reasons alone, the rejection based on Levitt is improper and should be withdrawn."

Examiner respectfully disagrees; applicant fails to give claim limitations the broadest most reasonable interpretation. A hybrid circuit is a combination of two circuits. During programming the host controller and programming slot are connected to the hearing aid (Levitt col. 8 lines 25-30) and are therefore removably part of the hearing aid.

See above arguments for claims 13 and 20. The previous office action is reinstated.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1-3, 9-10, and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749 in view of Madaffari et al. (2002/0090102).

Claim 1, Levitt discloses a transducer for coupling acoustic energy between an outside of the housing and an inside of the housing (Fig. 2: microphone 57, col. 4 line 64); and a hybrid circuit partially enclosed within the housing (Fig. 2), the hybrid circuit a first input circuit for coupling a signal from the transducer (Fig. 2: element 58); a filter network (Fig. 2: element 64) coupled to the first input circuit; an output circuit coupled to the filter network (col. 5 line 7-11); a tuner for adjusting the filter network(Fig. 2; 84 :EEPROM, tri-state switches, 85-86); and a controller for altering a value of the tuner(Fig. 1 host controller), the controller having a second input on the removable portion (Fig. 1:element 124 EEPROM socket), and a tuning signal coupled to the second input used to adjust the tuner, thereby changing a characteristic of the filter network (col. 2 line 49-51)

Levitt does not explicitly disclose the removable portion being removed after the characteristic of the filter network is changed.

However, Levitt discloses a removable portion used to program the characteristic of the filter (col. 5 line 1-5 and col. 6 line 59-62 and col. 8 line 25-30). It would be obvious to one of ordinary skilled in the art at the time the invention was made that the computer would be disconnected once programming is complete so that the user would not have to carry the programming unit.

Levitt does not disclose a housing having an acoustic seal and wherein the housing is acoustically sealed upon and by the removal of the removable portion.

Madaffari discloses a housing having an acoustic seal (Fig. 2, paragraph 15 line 13-15). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the housing of Madaffari in order to protect the circuit from EMI and other interferences. In addition it would be obvious to one of ordinary skill in the art at the time the invention was made to modify to seal the device immediately after programming in order to protect the circuitry from EMI and other interferences.

Claim 2 analyzed with respect to claim 1, Levitt further discloses, wherein the controller retains a setting upon receiving the tuning signal (col. 4 line 38-43).

Claim 3 analyzed with respect to claim 1, Levitt further discloses, wherein the removable portion is permanently removed after the controller receives the tuning signal (col. 8 line 25-29 the computer is disconnected after programming).

Claim 9 analyzed with respect to claim 1, Levitt further discloses wherein the second input is coupled to a biasing element, the biasing element maintaining a state after receiving the tuning signal (col. 5 line 34-37).

Claim 10 analyzed with respect to claim 1, Levitt further discloses wherein the transducer is a microphone (Fig. 2: element 57).

Claim 20, Levitt discloses, a transducer assembly having a transfer function of an acoustic energy to electrical energy comprising
a substrate having a first portion inside the housing (Fig. 2, col. 4 line 65) and a second portion removably attached to the first portion extending outside the housing (Fig. 1, host controller connected through EEPROM socket); and
a circuit disposed on the substrate for receiving a signal corresponding to acoustic energy received at the acoustic port (Fig. 2 col. 4 line 66-68),
whereby the transfer function of the miniature transducer assembly can be altered by a signal injected at the second portion of the substrate (col. 4 line 38-42).
Levitt does not explicitly disclose a second portion attached to the first portion. However Levitt discloses a second portion removably attached to the first portion (Fig. 1, host

controller connected through EEPROM socket). Therefore it would be obvious to one of ordinary skill in the art at the time the invention was made that during the programming of the hearing aid the EEPROM socket is attached to the hearing aid in order to download the necessary information.

Levitt does not disclose a housing comprising a first molded piece having an acoustic port; a second molded piece coupled to the first molded piece.

Madaffari discloses a housing comprising a first molded piece having an acoustic port (Fig. 2; element 52); a second molded piece coupled to the first molded piece (Fig. 2; element 42).

Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with the housing of Madaffari in order to protect the circuit from EMI and other interferences.

Claim 21 analyzed with respect to claim 20, Levitt further discloses wherein the second portion of the substrate is removably attached to the first portion (Fig. 1; EEPROM socket).

Claim 22 analyzed with respect to claim 20, Levitt further discloses wherein the circuit comprises a component for receiving the signal, the component operable to retain a programmed state after receiving the signal (Fig. 4 EEPROM col. 2 line 48-50).

Claim 23 analyzed with respect to claim 22 and 20, Levitt further discloses wherein the component is coupled to one of a resistor ladder network and a decoder (Fig. 4; element 148, col. 10 line 60-61).

Claim 24 analyzed with respect to claim 20, Levitt further discloses wherein the component is one of a zener-zap diode, an electrically erasable programmable read only memory (EEPROM), a poly-silicon fuse and a laser trimmable hybrid resistor (Fig. 4 EEPROM col. 2 line 48-50).

3. Claim 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749 in view of Madaffari et al. (2002/0090102) in further view of Killion (5602925).

Claim 4 analyzed with respect to claim 1, Levitt in view of Madaffari does not disclose wherein the tuner is a ladder network, the ladder network adjustable by activating or deactivating a semiconductor device between an element of the ladder network and a signal ground connection.

Killion discloses wherein the tuner is a ladder network, the ladder network adjustable by activating or deactivating a semiconductor device between an element of the ladder network and a signal ground connection (Fig. 6. col. 6 line 7-9). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt in view of Madaffari with the ladder network and semiconductor of

Killion in order to save space when implementing the circuit and in order to have a silicon based transistor that can be implemented with the rest of the circuit.

Claim 5 analyzed with respect to claim 4 and claim 1, Killion further discloses wherein the ladder network comprises resistors (Fig 6).

Claim 6 analyzed with respect to claim 5, 4 and 1, Killion further discloses wherein the resistors have a nominal value of 5.5k ohms. However, it would be obvious to one of ordinary skill in the art at the time the invention was made to set the value of the resistive element to 5.5k ohms in the course of circuit design so as to limit current applied or as necessary.

Claim 7 analyzed with respect to claim 4 and 1, Levitt further discloses wherein the ladder network comprises, capacitors (Fig. 4, col. 10 line 66-67).

Claim 8 analyzed with respect to claim 4, Killion further disclose wherein the semiconductor device is a field effect transistor (FET) (Fig.6 col. 6 line 7-9).

4. Claims 13, 15, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749) in view of in view of Madaffari et al. (2002/0090102) in further view of Sasaki et al (6294439)

Claim 13, Levitt discloses a portion of the buffer circuit accessible from outside the housing (Fig. 1; element 24);
providing a desired response characteristic for the buffer circuit (col. 6 line 65-67);
measuring an initial response characteristic of the buffer circuit (col. 6 line 68);
comparing the desired response characteristic to the initial response characteristic (col. 7 line 1-2); determining an adjustment using the comparison, the adjustment for reducing a difference between the desired and initial response characteristics (col. 7 line 1-2); transmitting a signal to a selector circuit in the buffer circuit (col. 7 line 6-8); and tuning an adjustable filter coupled to the selector circuit (col. 7 line 11-12), the adjustable filter for modifying the initial response characteristic (col. 7 line 65-67) and removing the portion of the buffer circuit accessible from outside the housing, the portion used in transmitting the signal to the selector circuit (col. 8 line 25-29, the computer is disconnected after programming.)

Levitt does not disclose assembling the buffer circuit in an acoustically sealed housing and wherein removing the portion of the buffer circuit along one of a scoring and line of weakness on a substrate carrying the buffer circuit.

Madaffari discloses assembling the buffer circuit in an acoustically sealed housing (Fig. 2, paragraph 15 line 13-15).

Therefore it would be obvious to one ordinarily skill in the art at the time the invention was made to modify the circuit of Levitt with the housing of Madaffari in order to protect the circuit from EMI and other interferences.

Levitt in view of Madaffari do not disclose wherein removing the portion of the buffer circuit along one of a scoring and line of weakness on a substrate carrying the buffer circuit.

Sasaki discloses one of a scoring and line of weakness on a substrate carrying a circuit (abstract line 1-3).

Therefore it would be obvious to one of ordinary skill in the art at the time the invention was made to modify the manufacture of the circuit of Levitt to include the grooves of Sasaki in order to have a circuit that can be easily integrated to with various other circuits.

Claim 15 analyzed with respect to claim 11, Levitt further discloses wherein the tuning the adjustable filter further comprises biasing the selector circuit with a biasing component (col. 5 line 34-40).

Claim 17 analyzed with respect to claim 15 and 11, Levitt further discloses wherein the biasing component is an electrically erasable programmable read-only memory (EEPROM) (col. 2 line 49-52).

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over over Levitt et al (4879749) in view of in view of Madaffari et al. (2002/0090102) in view of Sasaki et al (6294439) in further view of Killion (5602925).

Claim 14 analyzed with respect to claim 13, Levitt in view of Madaffari and Sasaki do not disclose wherein the tuning the adjustable filter further comprises activating a semiconductor device between an element of a ladder network and a ground connection.

Killion discloses wherein the tuning the adjustable filter further comprises activating a semiconductor device between an element of a ladder network and a ground connection (Fig. 6. col. 6 line 7-9). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt in view of Madaffari with the ladder network and semiconductor of Killion in order to save space when implementing the circuit and in order to have a silicon based transistor that can be implemented with the rest of the circuit.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749 in view of Madaffari et al. (2002/0090102) in view of Sasaki et al (6294439) and in further view of Advani et al. (4926459).

Claim 16 analyzed with respect to claim 15 and claim 13, Levitt in view of Madaffari and Sasaki do not disclose wherein the biasing component is a zener-zap diode.

Advani discloses wherein the biasing component is a zener-zap diode (Fig. 3; element 106, col.7 line 46-47). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the circuit of Levitt with a zener-zap diode as taught by Advani in order to utilize the breakdown characteristic of diodes.

7. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749 in view of in view of Madaffari et al. (2002/0090102) in view of Sasaki et al (6294439) in further view of Suzuki (5365768).

Claim 18 analyzed with respect to claim 15 and 13, Levitt in view of Madaffari and Sasaki do not disclose wherein the biasing component is a polysilicon fuse.

Suzuki discloses wherein the biasing component is a polysilicon fuse (col. 6 line 56-59).

Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the tuning circuit of Levitt in view of Madaffari with a polysilicon fuse, as taught by Suzuki so that the melting or nonmelting of the polysilicon fuse can be used as a digital memory (Suzuki col. 8 line 12-13).

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levitt et al (4879749 in view of Madaffari et al. (2002/0090102) in view of Sasaki et al (6294439) in further view of Lai (6229428).

Claim 19 analyzed with respect to claim 15 and claim 13, Levitt in view of Madaffari and Sasaki do not disclose wherein the biasing component is a laser trimmable hybrid resistor.

Lai discloses wherein the biasing component is a laser trimmable hybrid resistor (col. 1 line 65-66 and col. 2 line 48-49). Therefore it would be obvious to one ordinarily skilled in the art at the time the invention was made to modify the tuning circuit of Levitt in view

of Madaffari with a laser trimmable hybrid resistor, as taught by Lai in order to have a resistor that can still be adjusted after the circuit has been assembled.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FATIMAT O. OLANIRAN whose telephone number is (571)270-3437. The examiner can normally be reached on M-F 10:00-6 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on 571-272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FO

/Vivian Chin/
Supervisory Patent Examiner, Art Unit 2614